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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/435,766	11/08/99	KUSHIDA T	104361

MM92/1004

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EXAMINER	
LOKE,S	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 10/04/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/435,766	Applicant(s) Kushida
	Examiner Loke	Group Art Unit 2811

☐ Responsive to communication(s) filed on _____.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) 1-15 is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-15 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☒ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☒ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 2

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

2. The disclosure is objected to because of the following informalities:

In page 3, line 17, it is unclear whether fig. 8 is a cross-sectional view of a semiconductor device.

Appropriate correction is required.

3. Claims 1-11 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The specification never discloses how a bipolar transistor has a drain electrode, a drain region, a source electrode and a source region as claimed in claim 1.

4. Claims 11-15 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The specification never discloses the source region is located substantially at a center of the channel region and the source region is isolated from the insulation film for the embodiment of claim 1 as claimed in claim 11.

The specification never discloses a depletion layer forms over the entire channel region sandwiched between the gate region when a zero bias is applied to the gate region as claimed in claim 12.

The specification never discloses the source region is located substantially at a center of the channel region and the source region is isolated from the insulation film for the embodiment of claim 12 as claimed in claim 13.

The specification never discloses an impurity concentration in the channel region is equal to or less than an impurity concentration in the cathode region as claimed in claim 14.

The specification never discloses the anode includes an anode electrode that forms a Schottky junction with the channel as claimed in claim 15.

5. Claims 7-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 7, line 3, "an end face thereof" is unclear as to where is the end face.

In claim 9, line 4, "a space of the gate region" is unclear whether it is being referred to "a distance between the gate electrodes".

In claim 10, line 2, "the conductive layer" has no antecedent basis; lines 4-5, "the space of the gate region" is unclear whether it is being referred to "the distance between the gate electrodes".

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1 and 3 insofar, as in compliance with 35 USC 112, are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Terashima.

Terashima shows all the elements of the claimed invention in fig. 22. It comprises: an electrode [10]; a p-type region [2] and an n- type region [1] formed on the electrode [10]; a trench type insulated gate electrode [6] provided so as to surround at least a part of the channel region formed by the n- type region [1]; an n+ type region [4] and a p+ type region [20] formed on the channel region; an electrode [9] formed on the regions [4, 20]; a depletion layer is formed over most of the entire channel region when a predetermined voltage is applied to the gate electrode (col. 8, lines 5-16).

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 2 and 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Terashima.

In regards to claim 2, it would have been obvious for the gate region has the first conductive type because it is a well known gate electrode material for trench type vertical MOSFET.

In regards to claims 5 and 6, it would have been obvious for the source electrode forms a Schottky junction with the channel region because it is a well known contact structure for vertical MOSFET.

10. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Terashima in view of Ajit.

Terashima differs from the claimed invention by not having a source region formed at a center of the channel region.

Ajit shows a p+ type region [18] formed at a center of the channel region and is isolated from the insulated gate electrode [10] in fig. 15.

Since both Terashima and Ajit teach a vertical MOSFET with an n- type channel region and a p-type substrate, it would have been obvious to one of ordinary skills in the art to have the p+ type region of Ajit in Terashima because it improves breakdown voltage and reduces leakage current.

11. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams et al.

Williams et al. discloses a vertical MOSFET in figs. 10 and 11. It comprises: an n++ type region [101] and an n-type region [102]; a trench type insulated gate electrode [6] provided so as to surround at least a part of a p-type channel region [107]; an n+ type region [106] formed on the channel region.

It is well known in the art that a depletion layer is formed over most of the entire channel region sandwiched between the gate electrode when a zero bias is applied to the gate electrode.

It would have been obvious to have a source region formed at a center of the channel region and isolated from the insulation film because it improves breakdown voltage and reduces leakage current.

12. Claims 14 and 15 insofar, as in compliance with 35 USC 112, are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Mehrotra et al.

Mehrotra et al. shows all the elements of the claimed invention in fig. 5. It comprises: an n+ type cathode region [12c]; an n-type channel region [12d, 14] formed on the cathode region; an n-type anode region (the upper portion of region [14]) formed on the channel region; an impurity concentration of the channel region [12d, 14] is less than that of the cathode region [12c]; a Schottky junction is formed between the anode electrode [18] and the channel region [14].

13. Claims 7-10 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (703) 308-4920.

sl

October 1, 2000

STEVEN H. LOKE
PRIMARY EXAMINER
GROUP 2800

Steven Loke